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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,180	10/23/2001	Joseph D. Wert	P05023	6362

7590 09/12/2003

Docket Clerk
P.O. Drawer 800889
Dallas, TX 75380

EXAMINER
LAM, TUAN THIEU

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,180	WERT, JOSEPH D.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-13 and 17-22* is/are rejected.

7)☒ Claim(s) *3-5 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *18 August 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☑ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This is a response to the amendment filed 8/18/2003. Claims 1-22 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 6-13 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's cited prior art figure 2 in view of Takahashi (USP4,948,995), prior art of record.

Applicant's cited prior art figure 2 shows a power monitor circuit comprising first power supply (VDD), a second power supply VDDIO, wherein VDDIO > VDD, a voltage divider (205, 210), an odd number (one) of CMOS inverter (220, 225) for producing a status signal (OUT).

Applicant's cited prior art shows one CMOS inverter but does not (i) specify the odd number of serially connected CMOS inverters to be three or five; and (ii) status signal is an input signal to the voltage divider as called for in claims 1-2, 6-13 and 17-22.

Figure 3 of Takahashi reference shows a power supply monitoring circuit comprising an disabling transistor (14) receiving status signal DE and coupled to the detecting circuit (12, 13). The disabling transistor is to ensure there is no current is consumed in the detecting circuit and accordingly to reduce power consumption during the operation of integrated circuits. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to couple an disabling transistor to applicant's cited prior art voltage divider and for receiving the status signal in order to reduce power consumption in the voltage divider as taught by Takahashi.

Regarding the limitations of having the odd number of serially connected CMOS inverters to be three or five, although, applicant's cited prior art figure 2 shows only one CMOS inverter, it is well known more inverters would enhance the stability of the status signal thus prevent erroneous operations.

Response to Arguments

1. Applicant's arguments filed 8/18/2003 have been fully considered but they are not persuasive. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Takahashi teaches that power consumption can be reduced in the power on reset circuit by turning off the disabling circuit in the power on event. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to couple the disabling transistor to applicant's cited prior art voltage divider and for receiving the status signal in order to reduce power consumption in the voltage divider as taught by Takahashi.

2. Applicant argues that there would not have a reasonable expection of success for combining the applicant's cited prior art and Takahashi, given that the circuit of Takahashi uses a single power source is not persuasive. Applicant's cited prior art figure 2 has a draw back of a continuous current consumption when power supply VDDIO is on. Takahashi teaches that power consumption in the detecting circuit of the power on reset circuit can be eliminated by

inserting a disabling transistor (14). The disabling transistor is turned off when the power supply (15) is up thus no current is consumed in the detecting circuit and accordingly to reduce power consumption during the operation of integrated circuits. Thus, one skilled in the art would have recognized the benefits from the teaching Takahashi to insert a disabling transistor in the voltage divider to eliminate the current consumption. The same results are seen in a dual power supply in a power on reset circuit. Therefore, the rejection of claims 1-2, 6-13 and 17-22 is deemed to be proper.

Allowable Subject Matter

3. Claims 3-5 and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: none of the reference teach or suggest the limitations recited in claims 3 and 14.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

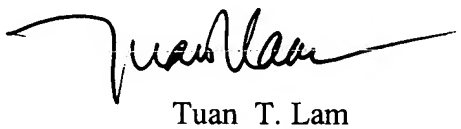
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 703-305-3791. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 730-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Tuan T. Lam
Primary Examiner
Art Unit 2816

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September 10, 2003